# DTU50P03

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# P-Channel 30 V (D-S) MOSFET

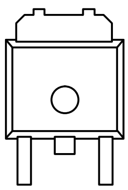
| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) Max. | $I_D$ (A) | $Q_g$ (Typ.) |
| - 30 | 0.016 at $V_{GS}$ = - 10 V | - 50[d] | 43.1 nC |
| | 0.022 at $V_{GS}$ = - 4.5 V | - 50[d] | |

## FEATURES

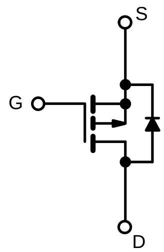
- DT-Trench Power MOSFET
- Low On-Resistance for Low Voltage Drop
- Extended $V_{GS}$ max. Rating: 25 V
- 100 % $R_g$ and UIS Tested

RoHS COMPLIANT

TO-252




Top View




P-Channel MOSFET

## APPLICATIONS

- Battery, Load and Adaptor Switches
  - Notebook Computers
  - Notebook Battery Packs

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | - 30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 25 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_C$ = 25 °C | $I_D$ | - 50[d] | A |
| | $T_C$ = 70 °C | | - 50[d] | |
| | $T_A$ = 25 °C | | - 23.1[a, b] | |
| | $T_A$ = 70 °C | | - 18.4[a, b] | |
| Pulsed Drain Current (t = 100 µs) | | $I_{DM}$ | - 300 | |
| Continuous Source-Drain Diode Current | $T_C$ = 25 °C | $I_S$ | - 50[d] | |
| | $T_A$ = 25 °C | | - 4.1[a, b] | |
| Avalanche Current | L = 0.1 mH | $I_{AS}$ | - 25 | |
| Single-Pulse Avalanche Energy | | $E_{AS}$ | 31.2 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | $P_D$ | 48 | W |
| | $T_C$ = 70 °C | | 31 | |
| | $T_A$ = 25 °C | | 5[a, b] | |
| | $T_A$ = 70 °C | | 3.2[a, b] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 150 | °C |
| Soldering Recommendations (Peak Temperature)[e, f] | | | 260 | |

## THERMAL RESISTANCE RATINGS

| Parameter | | Symbol | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient[a, c] | t ≤ 10 s | $R_{thJA}$ | 21 | 25 | °C/W |
| Maximum Junction-to-Case | Steady State | $R_{thJC}$ | 2.1 | 2.6 | |

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. Maximum under steady state conditions is 70 °C/W.

d. Package limited.

e. The TO-252 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

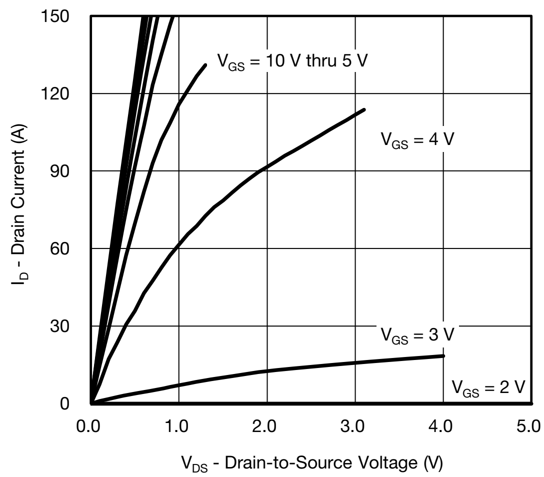
**SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0, $I_D$ = - 250 µA | - 30 | | | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = - 250 µA | | - 22 | | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | | 4.1 | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = - 250 µA | - 1.2 | | - 2.5 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 25 V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = - 30 V, $V_{GS}$ = 0 V | | | - 1 | µA |
| | | $V_{DS}$ = - 30 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | | | - 5 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS} \geq$ - 10 V, $V_{GS}$ = - 10 V | - 30 | | | A |
| Drain-Source On-State Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = - 10 V, $I_D$ = - 15 A | | 0.012 | 0.016 | Ω |
| | | $V_{GS}$ = - 4.5 V, $I_D$ = - 10 A | | 0.018 | 0.022 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = - 10 V, $I_D$ = - 15 A | | 60 | | S |
| **Dynamic[b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = - 15 V, $V_{GS}$ = 0 V, f = 1 MHz | | 5125 | | pF |
| Output Capacitance | $C_{oss}$ | | | 615 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 554 | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = - 15 V, $V_{GS}$ = - 10 V, $I_D$ = - 10 A | | 90 | 135 | nC |
| | | $V_{DS}$ = - 15 V, $V_{GS}$ = - 4.5 V, $I_D$ = - 10 A | | 43.1 | 65 | |
| Gate-Source Charge | $Q_{gs}$ | | | 13.6 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 28.8 | | |
| Gate Resistance | $R_g$ | f = 1 MHz | 0.5 | 2.4 | 4.8 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = - 15 V, $R_L$ = 1.5 Ω<br>$I_D \cong$ - 10 A, $V_{GEN}$ = - 10 V, $R_g$ = 1 Ω | | 15 | 30 | ns |
| Rise Time | $t_r$ | | | 12 | 24 | |
| Turn-Off DelayTime | $t_{d(off)}$ | | | 58 | 110 | |
| Fall Time | $t_f$ | | | 12 | 24 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = - 15 V, $R_L$ = 1.5 Ω<br>$I_D \cong$ - 10 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 1 Ω | | 60 | 120 | |
| Rise Time | $t_r$ | | | 60 | 120 | |
| Turn-Off DelayTime | $t_{d(off)}$ | | | 52 | 100 | |
| Fall Time | $t_f$ | | | 26 | 52 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continous Source-Drain Diode Current | $I_S$ | $T_C$ = 25 °C | | | - 50 | A |
| Pulse Diode Forward Current (100 µs) | $I_{SM}$ | | | | - 300 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = - 3 A, $V_{GS}$ = 0 | | - 0.74 | - 1.20 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = - 10 A, dI/dt = 100 A/µs, $T_J$ = 25 °C | | 23 | 46 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | 12 | 24 | nC |
| Reverse Recovery Fall Time | $t_a$ | | | 9 | | ns |
| Reverse Recovery Rise Time | $t_b$ | | | 14 | | |

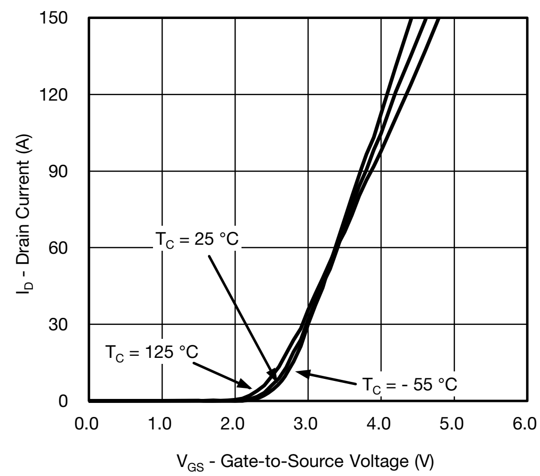
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

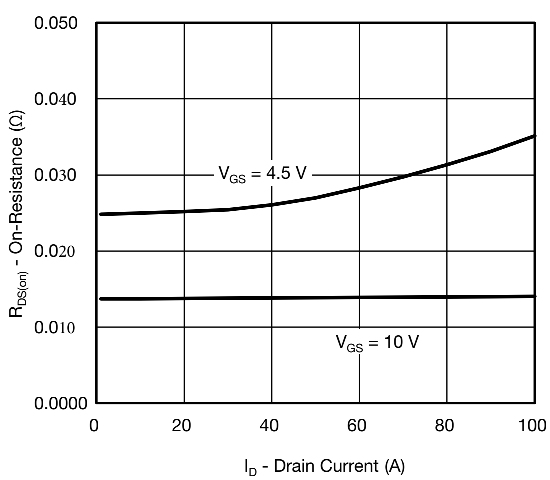
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



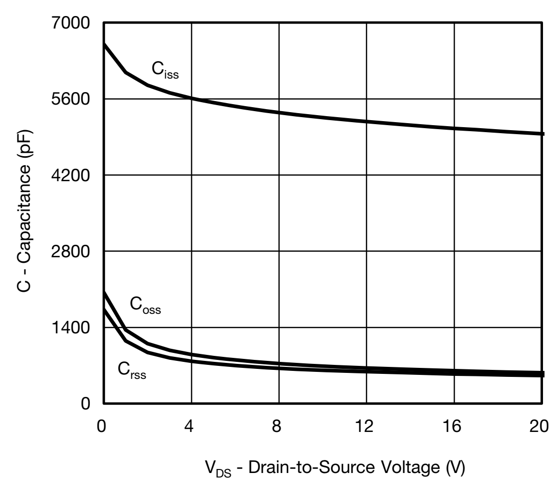

**Output Characteristics**



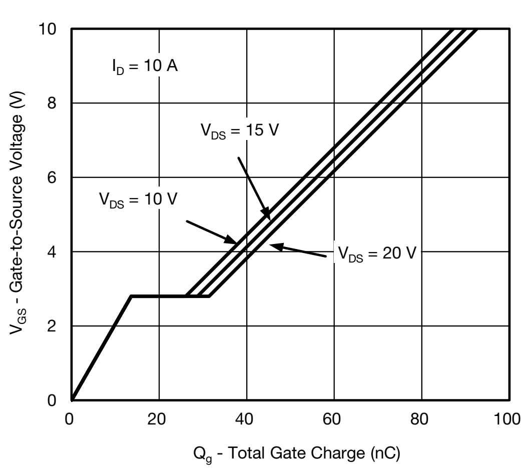

**Transfer Characteristics**



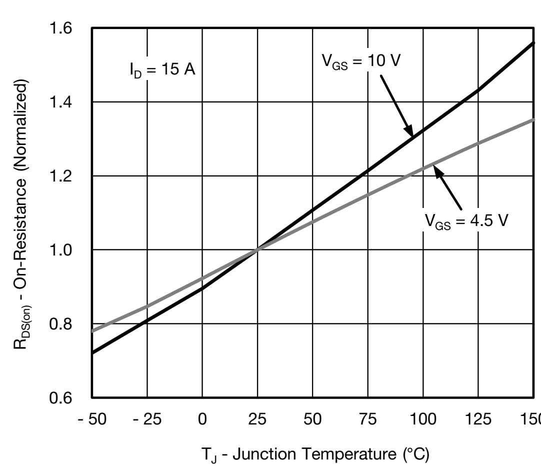

**On-Resistance vs. Drain Current**




**Capacitance**

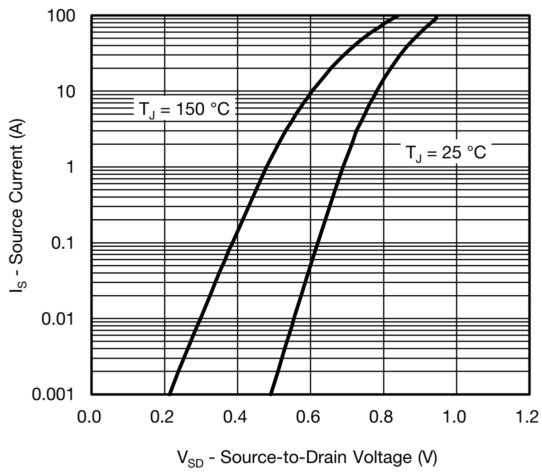



**Gate Charge**

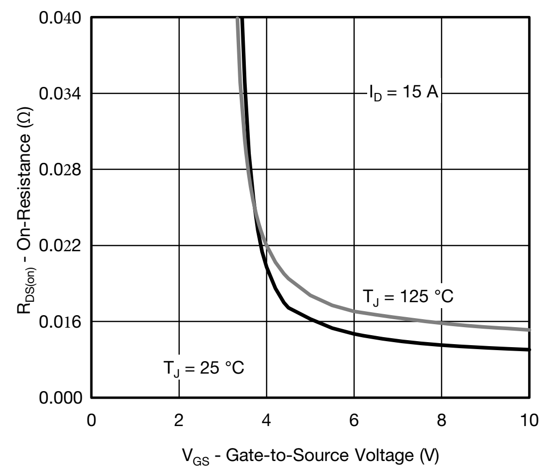



**On-Resistance vs. Junction Temperature**

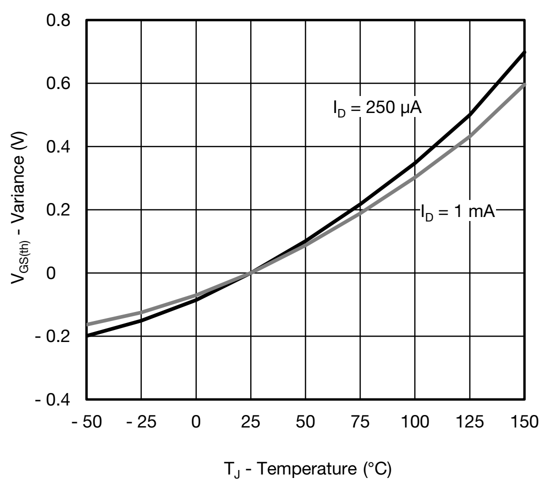
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



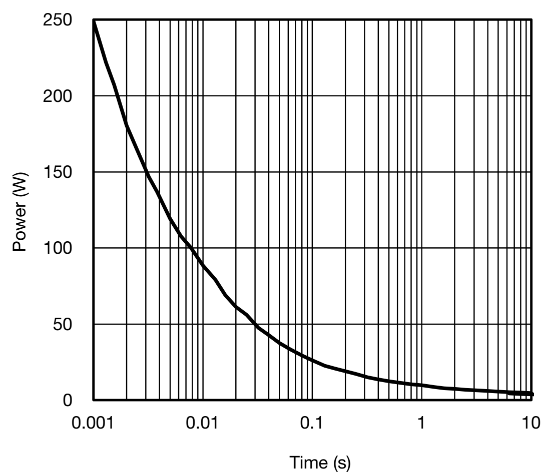

**Source-Drain Diode Forward Voltage**



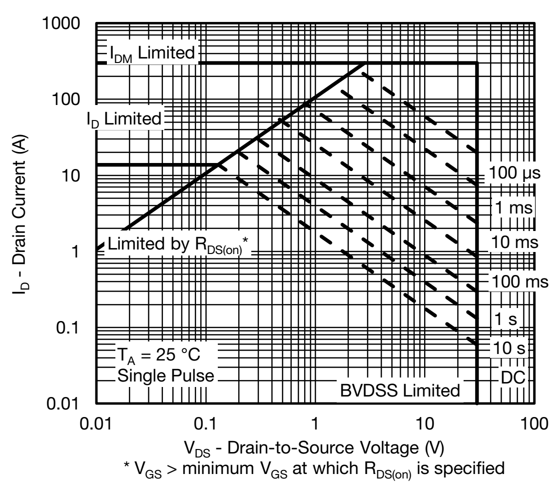

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**

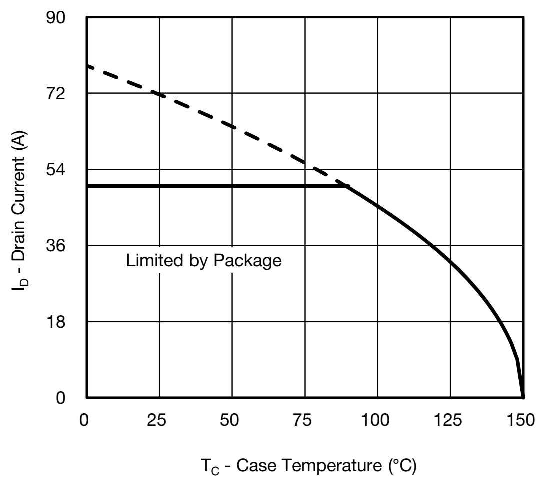



**Single Pulse Power, Junction-to-Ambient**

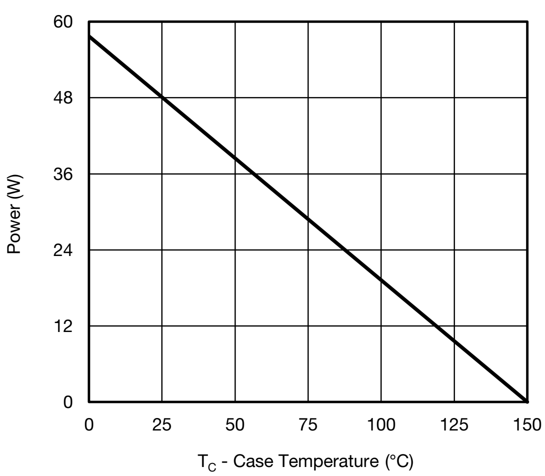



**Safe Operating Area**

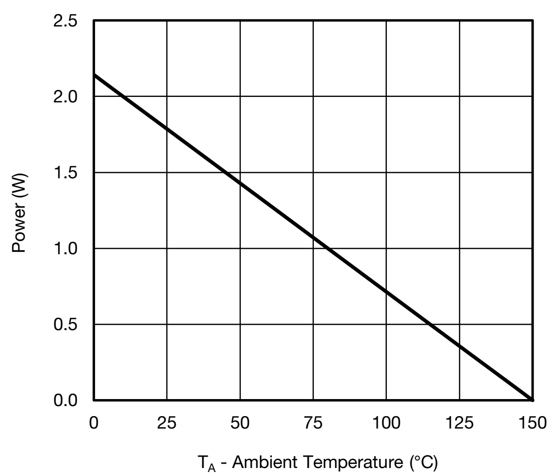
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)




**Current Derating***



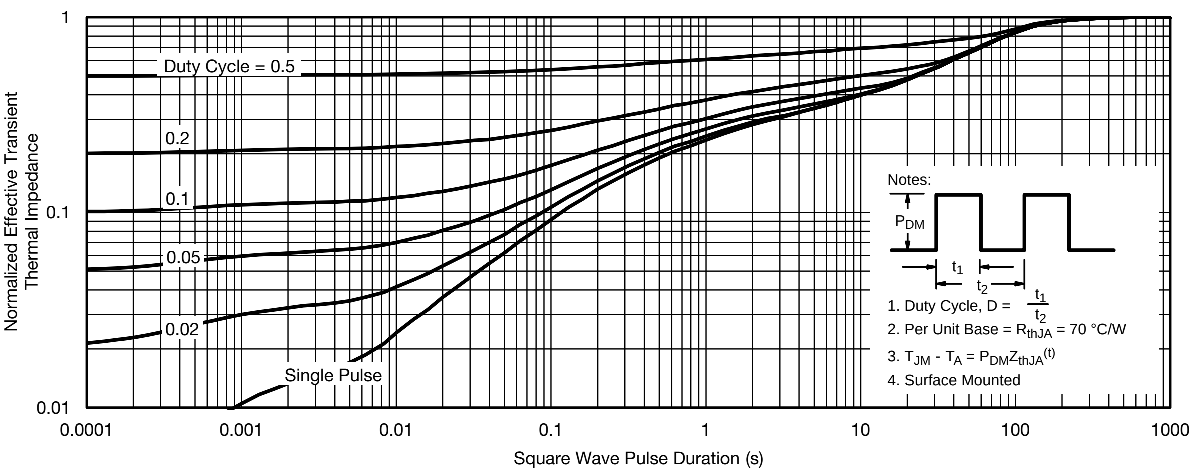

**Power, Junction-to-Case**



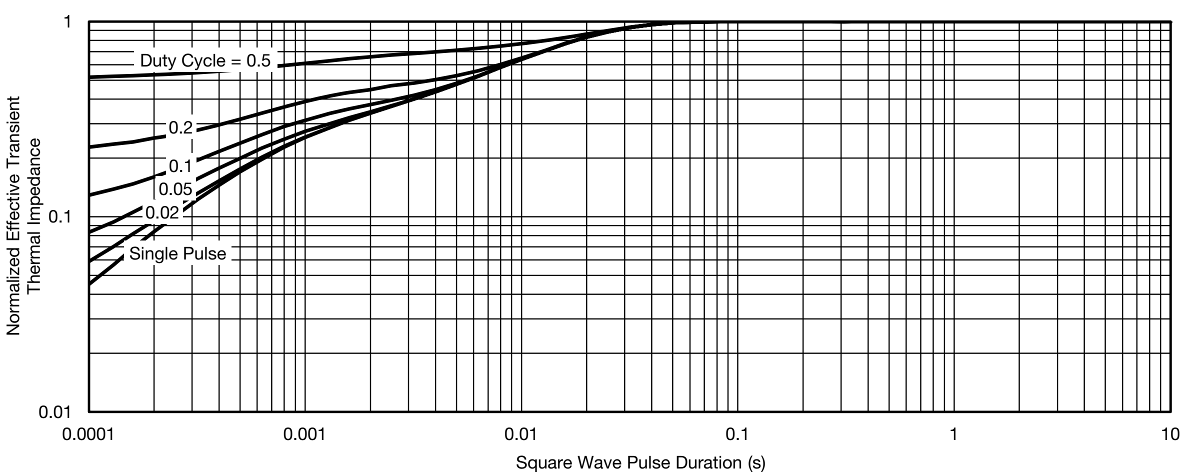

**Power Derating, Junction-to-Ambient**

* The power dissipation $P_D$ is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)




**Normalized Thermal Transient Impedance, Junction-to-Ambient**




**Normalized Thermal Transient Impedance, Junction-to-Case**

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